CLAIMS

What is claimed is:

1. A supply noise compensation circuit sensing the onset of noise events on a supply line and selectively gating off/forcing on a chip clock to chip circuits.

2. A supply noise compensation circuit as in claim 1 comprising:

supply noise sensing means for sensing the onset of noise events on a supply line;

means for synchronizing a clock skip signal from said supply noise sensing means to a chip clock; and

clock gating means for selectively gating said chip clock responsive to a synchronized said clock skip signal.

3. A supply noise compensation circuit as in claim 2 wherein said supply noise sensing means comprises:

a local clock buffer receiving said chip clock and providing a local clock;

a delay line receiving said local clock, said local clock propagating along said delay line, supply line noise affecting propagation of said clock along said delay line; and

a register latching delay line tap contents responsive to said local clock, latched tap locations indicating propagation of said clock in said delay line.

4. A supply noise compensation circuit as in claim 3 wherein said delay line is at least 3 global clock cycles long.

5. A supply noise compensation circuit as in claim 4 wherein said delay line taps are evenly spaced along said delay line and a clock edge in said delay line is identified by a matched state at a pair of adjacent said delay line taps.

6. A supply noise compensation circuit as in claim 4 wherein said local clock is a pair of complementary clock phases.

7. A supply noise compensation circuit as in claim 4 wherein said delay line is a number (N) of series connected inverters.

8. A supply noise compensation circuit as in claim 7 wherein said register is an N bit register, each bit receiving an output of one of said series connected inverters.

9. A supply noise compensation circuit as in claim 4 wherein said sensing means further comprises a compare comparing adjacent bits in said register, identifying a change in timing edge spacing and providing a skip signal.

10. A supply noise compensation circuit as in claim 9 wherein said clock gating means receives said skip signal and selectively passes said chip clock responsive to said skip signal.

11. A supply noise compensation circuit as in claim 10 wherein said clock gating means selectively prevents pausing distribution of said chip clock responsive to said skip signal, thereby forcing presentation of said on chip clock to respective said chip clock circuits.

12. A supply noise compensation circuit as in claim 10 wherein said synchronizing means comprises said register and said clock gating means.

13. A supply noise compensation circuit as in claim 2 wherein said supply noise sensing means comprises:

means for averaging supply line voltage; and

means for comparing instantaneous said supply line voltage against an average said supply line voltage.

14. A supply noise compensation circuit as in claim 12 wherein said means for synchronizing comprises a latch.

15. A supply noise compensation circuit as in claim 12 wherein said clock gating means is an AND gate ANDing a compare output from said means for comparing and said chip clock, an output of said AND gate being a gated clock.

16. A supply noise compensation circuit as in claim 1 wherein said noise events are dI/dt noise events.

17. An integrated circuit (IC) chip having a plurality of functional units distributed on said chip and in communication with each other, each of said functional units being supplied by a common voltage supply, said IC chip further including at least one supply noise compensation circuit sensing the onset of dI/dt noise events on said common voltage supply and selectively gating a chip clock to at least one chip circuit in at least one chip unit.

18. An IC chip as in claim 17, said supply noise compensation circuit comprising:

a delay line receiving a local clock, said local clock propagating along said delay line, supply line noise affecting propagation of said clock along said delay line;

a register latching delay line tap contents responsive to said local clock, latched tap locations indicating propagation of said clock in said delay line;

a compare comparing adjacent bits in said register and identifying a change in timing edge spacing and providing a clock skip signal; and

a clock skip circuit selectively gating said chip clock responsive to a said clock skip signal.

19. An IC chip as in claim 18, said supply noise compensation circuit further comprising:

a local clock buffer receiving said chip clock and providing a local clock.

20. An IC chip as in claim 19 wherein said local clock is a pair of complementary clock phases.

21. An IC chip as in claim 18 wherein delay line taps are evenly spaced along said delay line and a clock edge in said delay line is identified by a matched state at a pair of adjacent said delay line taps.

22. An IC chip as in claim 18 wherein said delay line is a number (N) of series connected inverters, nominal delay through said inverters being at least 3 clock cycles long.

23. An IC chip as in claim 22 wherein said register is an N bit register, each bit receiving an output of one of said series connected inverters.

24. An IC chip as in claim 18 wherein said clock skip circuit selectively prevents pausing distribution of said chip clock responsive to said skip signal, thereby forcing presentation of said on chip clock to respective said chip clock circuits.

25. An IC chip as in claim 17 wherein said at least one noise compensation circuit is a plurality of noise compensation circuits, each gating a global clock to a respective one of said units.

26. An IC chip as in claim 17, said supply noise compensation circuit comprising:

an RC filter averaging supply line voltage;

a comparator comparing instantaneous said supply line voltage against an average said supply line voltage; and

an AND gate gating said chip clock responsive to said comparing means.

27. An integrated circuit (IC) chip having a plurality of functional units distributed on said chip and in communication with each other, each of said functional units being supplied by a common voltage supply, said IC chip further including at least one supply noise compensation circuit sensing the onset of dI/dt noise events on said common voltage supply and selectively gating a chip clock to at least one chip circuit in at least one chip unit, said supply noise compensation circuit comprising:

a local clock buffer receiving said chip clock and providing a local clock;

a delay line receiving a local clock, said local clock propagating along said delay line, supply line noise affecting propagation of said clock along said delay line, nominal delay through said inverters being at least 3 clock cycles long;

an N bit register latching delay line tap contents responsive to said local clock, latched tap locations indicating propagation of said clock in said delay line;

a compare comparing adjacent bits in said register and identifying a change in timing edge spacing and providing a clock skip signal; and

a clock skip circuit selectively gating said chip clock responsive to a said clock skip signal.

28. An IC chip as in claim 27, wherein said delay line is N series connected inverters, each inverter output being a delay line tap and a clock edge in said delay line being identified by a matched state at a pair of adjacent delay line taps.

29. An IC chip as in claim 28 wherein said clock skip circuit selectively prevents pausing distribution of said chip clock responsive to said skip signal, thereby forcing presentation of said on chip clock to respective said chip clock circuits.

30. An IC chip as in claim 29 wherein said local clock is a pair of complementary clock phases.

31. An IC chip as in claim 30 wherein said at least one noise compensation circuit is a plurality of noise compensation circuits, each gating a global clock to a respective one of said units.